DEVICE FOR STORAGE OF MULTIPORT DATA, PARTICULARLY FOR AN ARITHMETIC AND LOGIC UNIT OF A DIGITAL SIGNAL PROCESSING PROCESSOR

Abstract of the Disclosure

The data storage device includes several registers that can be addressed by address words, and connected to p output ports through connections that can be configured in response to address words of p registers selected to read the contents of these registers on the p ports respectively. All register address words contain a specific bit with a predetermined rank identical for all address words and remaining bits. The registers are connected in pairs on each output port, each pair of registers containing two registers with address words that only differ in the value of the said specific bit. The connections include a pair of first switches that can be controlled in a complementary manner by the specific bit in the address word of one of the two registers, and a second switch connected to the output port considered and that can be controlled from the remaining bits of the address words of the two registers, for each pair of registers and for each output port, the first two switches are connected firstly between the corresponding two registers, and secondly between the corresponding second switch.